ABSTRACT OF THE DISCLOSURE

An input/output data pipeline circuit of a semiconductor memory device includes a first transmitting unit, a control signal generating unit, and a second transmitting unit. The first transmitting unit receives data stored in a memory cell and transmits data to an input/output driver in response to activation of a first switching signal and a second switching signal. The control signal generating unit receives a clock signal from the semiconductor memory device and, corresponding to the frequency of the clock signal, outputs a control signal, the first switching signal, and the second switching signal. The second transmitting unit transmits data to the input/output driver in response to activation of the control signal. The first transmitting unit and the second transmitting unit are alternatively activated.